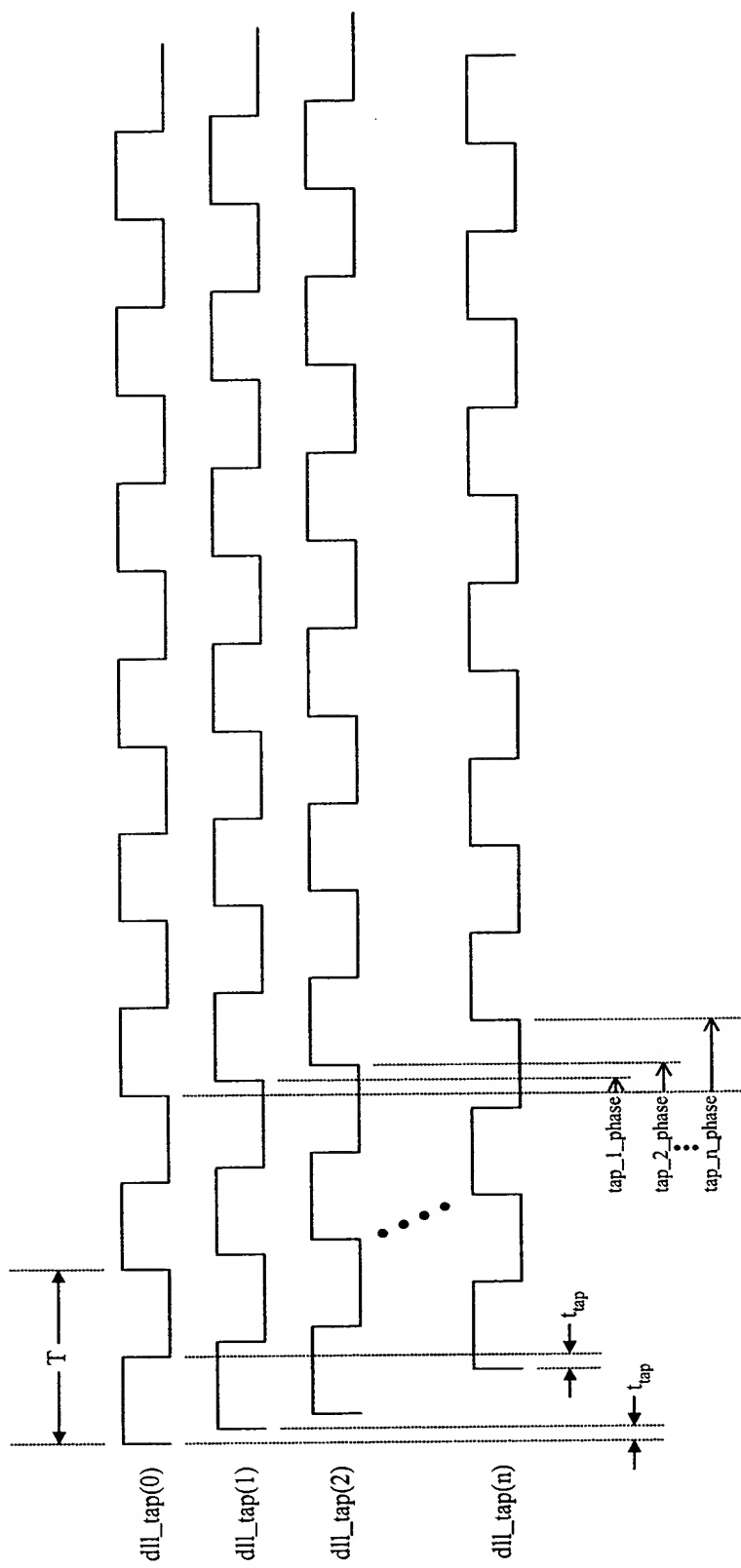


Fig. 1



$t_{tap} = (1 / [(n+1) * 2]) * T$ , where  $T$  = clock period,  $n$  = number of DLL taps =  $1/2$  the number of output clock offset/width positions within one period,  $T$ .

$tap\_0\_phase = t_{tap} * 0 = 0$

$tap\_1\_phase = t_{tap} * 1$

$tap\_2\_phase = t_{tap} * 2$

$\vdots$

$tap\_n\_phase = t_{tap} * n$

**Fig. 2**

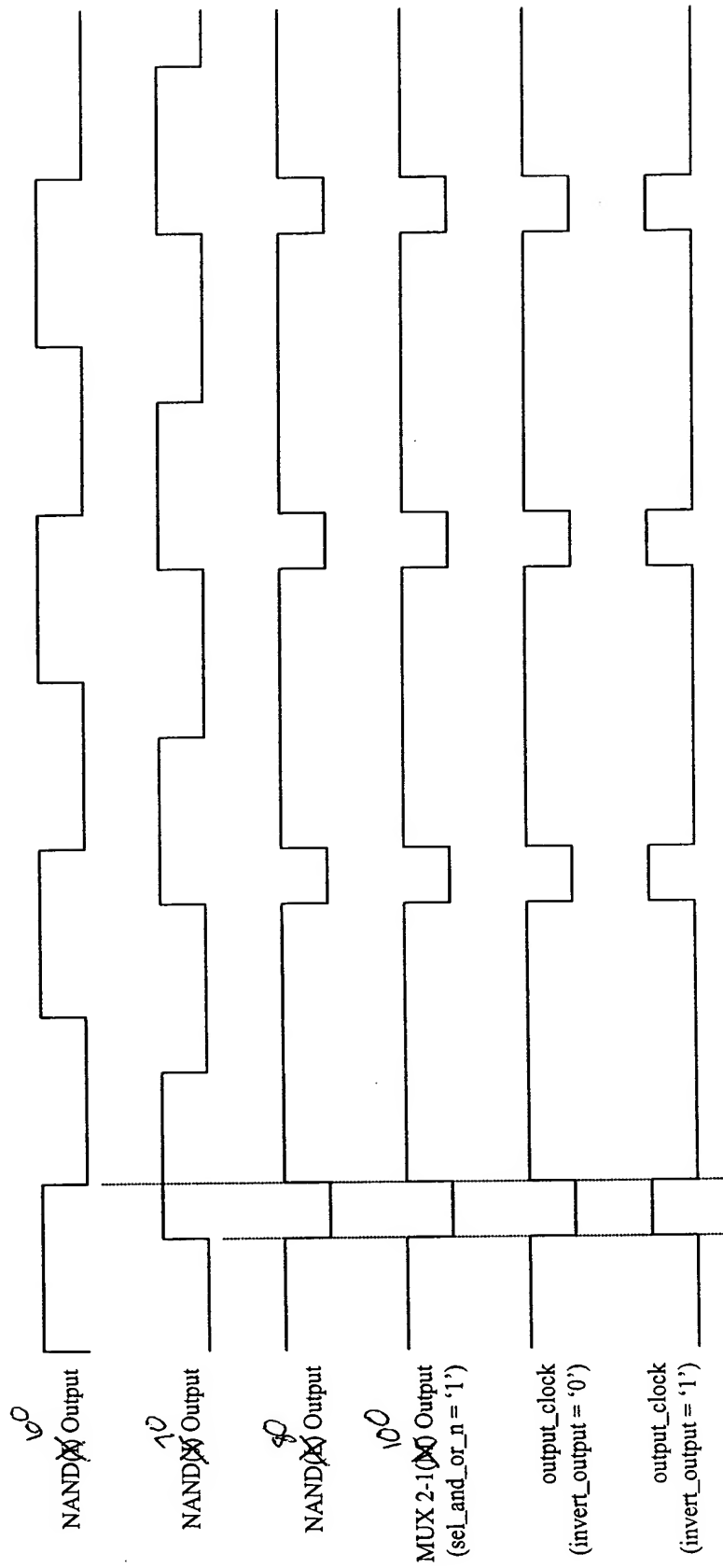


Fig. 3

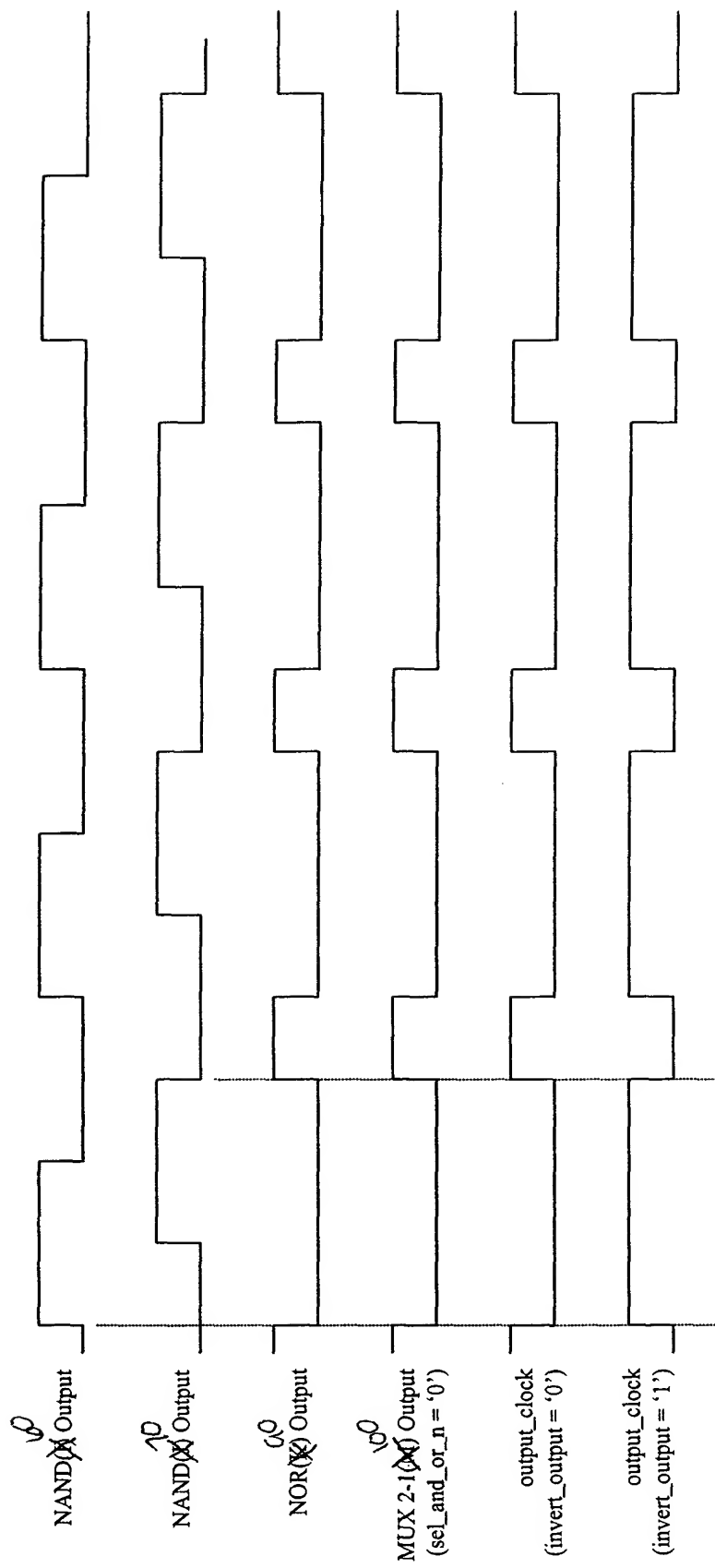


Fig. 4